IN THE CLAIMS:

Amend claims 1, 2, 5, 8, 12, 16 and cancel claims 6, 9, 13, 17-19, 21 and 23 without prejudice or admission as shown in the following listing of claims, which replaces all previous versions and listings of claims in this application.

1. (currently amended) A memory interface device for controlling memory access between a memory write unit that writes data into a memory and a memory readout unit that reads the data from the memory, the memory write unit being in compliance with a memory write procedure in which each time data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is performed, the memory interface device comprising:

write detection means for detecting a memory write procedure in which ~~the write of the predetermined unit amount of the data by~~ the memory write unit writes the predetermined unit amount of the data into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the write detection means, a readout completion notice signal ~~to notify~~ that notifies the memory write unit, and thereby confirms, that the readout of the data from the memory by the memory readout unit has been completed so that the memory write unit

proceeds to perform a next memory write procedure of the data into the memory;

data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures;

memory readout control means for generating an interrupt signal ~~with respect to the memory readout unit~~ to temporarily stop the generation of the readout completion notice signal by the signal generation means when the stored data amount ~~in the memory~~ measured by the data storage amount measurement means reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data amount measured by the data storage amount measurement means; and

a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the memory readout control means when a value of the period count reaches a predetermined timer period, the memory readout control means generating and outputting the interrupt signal ~~with respect~~ to the memory readout unit even when the memory readout control means receives the timeout signal output from the timer.

2. (currently amended) A memory interface device for connection to a memory write unit to control a memory access to the memory write unit, the memory write unit being in compliance with a memory write procedure in which each time data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is performed, the memory interface device comprising:

write detection means for detecting a memory write procedure in which ~~the write of the predetermined unit amount of the data by~~ the memory write unit writes the predetermined unit amount of the data into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the write detection means, a readout completion notice signal ~~to notify~~ that notifies the memory write unit, and thereby confirms, that readout of the data from the memory has been completed so that the memory write unit proceeds to perform a next memory write procedure of the data into the memory;

data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures;

data processing means for reading the data from the memory and for subjecting the read data to predetermined processing;

memory readout control means for generating an interrupt signal ~~with respect to the data processing means~~ to temporarily stop the generation of th readout completion notice signal by the signal generation means when the stored data amount ~~in the memory~~ measured by the data storage amount measurement means reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the data processing means so that the data processing means reads out all of the data stored in the memory in accordance with the stored data amount measured by the data storage amount measurement means; and

a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the memory readout control means when a value of the period count reaches a predetermined timer period, the memory readout control means generating and outputting the interrupt signal ~~with respect~~ to the data processing means even when the memory readout control means receives the timeout signal output from the timer.

3.- 4. (canceled).

5. (currently amended) A memory interface method for controlling memory access between a memory write unit that writes data into a memory and a memory readout unit that reads the data from the memory, the memory write unit being in compliance with a

memory write procedure in which each time data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is performed, the memory interface method comprising:

a step of detecting a memory write procedure in which ~~the write of the predetermined unit amount of the data by~~ the memory write unit writes the predetermined unit amount of the data into the memory;

a step of generating, upon detection of the memory write procedure, a readout completion notice signal that notifies the memory write unit, and thereby confirms, that ~~notifying the memory write unit, upon detection of the writing of the predetermined unit amount of the data, that~~ the readout of the data from the memory by the memory readout unit has been completed so that the memory write unit proceeds to perform a next memory write procedure of the data into the memory;

a step of measuring an amount of the data stored in the memory during the memory write procedures;

a step of generating an interrupt signal to temporarily stop the generation of the readout completion notice signal ~~with respect to the memory readout unit~~ when the measured stored data amount ~~in the memory~~ reaches a predetermined readout start storage amount, and a step of outputting the interrupt signal to the memory readout unit so that the memory readout unit reads all

of the data stored in the memory in accordance with the measured stored data amount;

a step of counting a period in which writing of the predetermined unit amount of the data is discontinued and a step of outputting a timeout signal when a value of the period count reaches a predetermined count period; and

a step of generating and outputting the interrupt signal ~~with respect~~ to the memory readout unit when a value of the period count reaches a predetermined timer period.

6. - 7. (canceled).

8. (currently amended) A memory interface device for controlling memory access between a first memory write and readout unit and a second memory write and readout unit which write and read data with respect to a memory, the first memory write and readout unit being in compliance with a memory write procedure in which each time data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is performed, the memory interface device comprising:

first write detection means for detecting the write of the predetermined unit amount of the data by the first memory write and readout unit into the memory;

first completion signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the first write detection means, a completion signal to notify the first memory write and readout unit that the readout of the data from the memory has been completed;

first data storage amount measurement means for measuring an amount of the data stored in the memory during the memory write procedures;

first memory readout control means for generating an interrupt signal ~~with respect to the second memory write and readout unit~~ to temporarily stop the signal generation by the first completion signal generation means when the stored data amount in the memory reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the first memory write and readout unit so that the first memory write and readout unit reads out all of the data stored in the memory in accordance with the stored data amount measured by the first data storage amount measurement means;

second write detection means for detecting the write of the predetermined amount of the data from the second memory write and readout unit into the memory;

second completion signal generation means for generating, upon detection of the writing of the predetermined unit amount of the data by the second write detection means, a

completion signal to notify the first memory write and readout unit that the write of the data into the memory has been completed;

second data storage amount measurement means for measurement the stored data amount in the memory during the memory write procedures;

second memory readout control means for generating an interrupt signal with respect to the second memory write and readout unit when the stored data amount in the memory reaches a predetermined readout completion storage amount; and

a first timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the first memory readout control means when a value of the period count reaches a predetermined timer period, the first memory readout control means generating the interrupt signal with respect to the second memory write and readout unit even when the first memory readout control means receives the timeout signal output from the first timer.

9. - 11. (canceled).

12. (currently amended) A memory interface method for controlling memory access between a first memory write and readout unit and a second memory write and readout unit which write and read data with respect to a memory, the first memory

write and readout unit being in compliance with a memory write procedure in which each time data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next memory write procedure of the data into the memory is performed, the memory interface method comprising:

a step of detecting the write of the predetermined unit amount of the data from the first memory write and readout unit into the memory;

a step of notifying the first memory write and readout unit, upon detection of the predetermined unit amount of the data, that the readout of the data from the memory has been completed;

a step of measuring an amount of the data stored in the memory as a result of the ~~memory write procedures~~ detected write of the predetermined unit amount of data from the first memory write and readout unit into the memory;

a step of generating an interrupt signal with respect to the ~~second~~ first memory write and readout unit to temporarily stop notification to the first memory write and readout unit of the completion of the readout of the data from the memory when the measured stored data amount in the memory reaches a predetermined readout start storage amount, and a step of outputting the interrupt signal to the first memory write and readout unit so that the first memory write and readout unit

reads out all of the data stored in the memory in accordance with the measured stored data amount;

a step of detecting the write of the predetermined unit amount of the data from the second memory write and readout unit into the memory;

a step of generating a signal, upon detection of the writing of the predetermined unit amount of data, to notify the first memory write and readout unit that the write of the data into the memory has been completed;

a step of measuring the stored data amount in the memory as a result of the detected writing of the predetermined unit amount of data from the second memory write and readout unit into the memory;

a step of generating an interrupt signal with respect to the second memory write and readout unit when the stored data amount in the memory reaches a predetermined readout completion storage amount;

a step of counting a period in which the write of the predetermined unit amount of the data is discontinued; and

a step of generating the interrupt signal with respect to the second memory write and readout unit when the a value of the period count reaches a predetermined timer period.

13. - 15. (canceled).

16. (currently amended) A modem device for connection to a data processing unit that complies with a memory write procedure in which each time communication data or control command data is written into a memory by a predetermined unit amount, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed, the modem device comprising:

a modem interface that exchanges communication data or control command data with respect to the data processing unit;

a memory into which the communication data or control command data is written;

a memory readout unit that reads the communication data or control command data from the memory;

communication means connected to the memory readout unit to transmit and receive the communication data or the control command data;

write detection means for detecting the write of the predetermined unit amount of the communication data or the control command data from the data processing unit into the memory;

signal generation means for generating, upon detection of the writing of the predetermined unit amount of the communication data or the control command data, a readout completion notice signal ~~to notify~~ that notifies the data processing unit, and thereby confirms, that the readout of the

communication data or the control command data from the memory has been completed so that the data processing unit proceeds to perform a next write procedure into the memory;

data storage amount measurement means for measuring an amount of the communication data or the control command data stored in the memory;

memory readout control means for generating an interrupt signal ~~with respect to the memory readout unit~~ to temporarily stop the generation of the readout completion notice signal when the stored data amount in the memory reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data mount measured by the data storage amount measurement means; and

counting means for counting a period in which writing of the predetermined unit amount of the data into the memory is discontinued and for outputting a timeout signal to the memory readout control means when a predetermined value of the period count is reached, the memory readout control means generating and outputting the interrupt signal ~~with respect~~ to the memory readout unit even when the memory readout control means receives the timeout signal.

17. - 19. (canceled).

20. (previously presented) A memory interface device according to claim 8; further comprising a second timer that counts a period in which the write of the data from the second memory write and readout unit into the memory is discontinued when a value of the period count reaches a predetermined timer period, the second timer outputting a timeout signal to the second completion signal generation means; and wherein the second completion signal generation means generates a completion notice signal with respect to the first memory write and readout unit upon receipt of the timeout signal.

21. (canceled).

22. (previously presented) A memory interface method according to claim 12; further comprising: a step of counting a period in which the write of the data from the second memory write and readout unit into the memory is discontinued; a step of outputting a timeout signal when a value of the period count reaches the predetermined timer period; and a step of outputting a completion signal to the first memory write and readout unit in response to the timeout signal.

23. (canceled).